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APPLICATION FOR LETTERS PATENT

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**Method Of Depositing An Aluminum Nitride
Comprising Layer Over A Semiconductor Substrate,
Method Of Forming DRAM Circuitry, DRAM
Circuitry, Method Of Forming A Field Emission
Device, And Field Emission Device**

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1 Method Of Depositing An Aluminum Nitride Comprising Layer Over
2 A Semiconductor Substrate, Method Of Forming DRAM Circuitry,
3 DRAM Circuitry, Method Of Forming A Field Emission Device, And
4 Field Emission Device

5 TECHNICAL FIELD

6 This invention relates to methods of depositing aluminum nitride
7 comprising layers over semiconductor substrates, to methods of forming
8 DRAM circuitry, to DRAM circuitry, to methods of forming field
9 emission devices, and to field emission devices.

10 BACKGROUND OF THE INVENTION

11 This invention was principally motivated in addressing problems
12 and improvements in dynamic random access memory (DRAM) and in
13 field emission devices, such as displays.

14 As DRAMs increase in memory cell density, there is a continuing
15 challenge to maintain sufficiently high storage capacitance despite
16 decreasing cell area. Additionally, there is a continuing goal to further
17 decrease cell area. One principal way of increasing cell capacitance is
18 through cell structure techniques. Such techniques include
19 three-dimensional cell capacitors, such as trench or stacked capacitors.
20 Yet as feature size continues to become smaller and smaller,
21 development of improved materials for cell dielectrics as well as the cell
22 structure are important. The feature size of 256Mb DRAMs will be on
23 the order of 0.25 micron or less, and conventional dielectrics such as
24

1 SiO₂ and Si₃N₄ might not be suitable because of small dielectric
2 constants. Highly integrated memory devices, such as 256 Mbit DRAMs
3 and beyond, are expected to require a very thin dielectric film for the
4 3-dimensional capacitor of cylindrically stacked or trench structures. To
5 meet this requirement, the capacitor dielectric film thickness will be
6 below 2.5nm of SiO₂ equivalent thickness.

7 Field emission displays are one type of field emission device, and
8 are utilized in a variety of display applications. Conventional field
9 emission displays include a cathode plate having a series of emitter tips
10 fabricated thereon. The tips are configured to emit electrons toward
11 a phosphor screen to produce an image. The emitters are typically
12 formed from an emitter material such as conductive polysilicon,
13 molybdenum, or aluminum. Multiple emitters are typically utilized to
14 excite a single pixel. For example, 120 emitters may be used for a
15 single pixel. Individual pixels contain a deposited one of red, green,
16 or blue phosphor.

17 Clarity, or resolution, of a field emission display is a function of
18 a number of factors, including emitter tip sharpness. Specifically,
19 sharper emitter tips can produce higher resolution displays than less
20 sharp emitter tips. One adverse phenomenon impacting emitter tip
21 sharpness is undesired native oxidation of the emitter tips during
22 fabrication if exposed to an oxidizing atmosphere, such as room air.
23 Such oxidation consumes material of the tips in forming an oxide and
24 reduces sharpness and therefore clarity.

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SUMMARY OF INVENTION

The invention is a method of depositing an aluminum nitride comprising layer over a semiconductor substrate, a method of forming DRAM circuitry, DRAM circuitry, a method of forming a field emission device, and a field emission device. In one aspect, a method of depositing an aluminum nitride comprising layer over a semiconductor substrate includes positioning a semiconductor substrate within a chemical vapor deposition reactor. Ammonia and at least one compound of the formula R_3Al , where "R" is an alkyl group or a mixture of alkyl groups, are fed to the reactor while the substrate is at a temperature of about 500°C or less and at a reactor pressure from about 100 mTorr to about 725 Torr effective to deposit a layer comprising aluminum nitride over the substrate at such temperature and reactor pressure. In one aspect, such layer is utilized as a cell dielectric layer in DRAM circuitry. In one aspect, such layer is deposited over emitters of a field emission display.

In one aspect, the invention includes DRAM circuitry having an array of word lines forming gates of field effect transistors and an array of bit lines. Individual field effect transistors have a pair of source/drain regions. A plurality of memory cell storage capacitors are associated with the field effect transistors. Individual storage capacitors have a first capacitor electrode in electrical connection with one of a pair of source/drain regions of one of the field effect transistors and a second capacitor electrode. A capacitor dielectric region is received

1 intermediate the first and second capacitor electrodes, with the region
2 comprising aluminum nitride, and the other of the pair of source/drain
3 regions of the one field effect transistor being in electrical connection
4 with one of the bit lines.

5 In one aspect, a field emission device includes an electron emitter
6 substrate including emitters having at least a partial covering comprising
7 an electrically insulative material other than an oxide of silicon, with
8 aluminum nitride being but one example. An electrode collector
9 substrate is spaced from the electron emitter substrate.

10 11 12 **BRIEF DESCRIPTION OF THE DRAWINGS**

13 Preferred embodiments of the invention are described below with
14 reference to the following accompanying drawings.

15 Fig. 1 is a diagrammatic sectional view of a semiconductor wafer
16 fragment comprising example DRAM circuitry in accordance with an
17 aspect of the invention.

18 Fig. 2 is a diagrammatic sectional view of an example field
19 emission device substrate having emitters in accordance with an aspect
20 of the invention.

21 Fig. 3 is a view of the Fig. 2 device at a processing step
22 subsequent to that shown by Fig. 2.

23 Fig. 4 is a schematic, sectional view of one embodiment of a field
24 emission display incorporating the example Fig. 3 substrate.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In one implementation of the invention, a semiconductor substrate is positioned within a chemical vapor deposition reactor. Ammonia and at least one compound of the formula R_3Al , where "R" is an alkyl group or a mixture of alkyl groups, is fed to the reactor while the substrate is at a temperature of about 500°C or less, and at a reactor pressure from about 100 mTorr to about 725 Torr, effective to deposit a layer comprising aluminum nitride over the substrate at such temperature and reactor pressure. Example compounds include those which have three of the same alkyl groups, such as triethylaluminum and trimethylaluminum, and those which have at least two different alkyl groups, for example methyldiethylaluminum, dimethylethylaluminum etc. Substrate temperature is preferably kept at greater than or equal to about 250°C, with from about 380°C to about 420°C being more preferred. Substrate temperature and reactor pressure are preferably maintained substantially constant during the feeding and deposit. Preferred reactor pressure is from about 10 Torr to about 100 Torr. Plasma is preferably not utilized, and the aluminum nitride is preferably substantially amorphous. In the context of this document, "substantially amorphous" is meant to define a material which is at least 90%

1 amorphous. Aluminum nitride layer deposition in these manners can
2 have reduced carbon and oxygen incorporation.

3 In a specific example, a liquid volume of triethylaluminum was
4 maintained at a temperature of 75°C. Helium was flowed through this
5 liquid at the rate of 100 sccm and into a chemical vapor deposition
6 chamber within which a semiconductor wafer was received and
7 maintained at the temperature of 450°C. Ammonia was also flowed to
8 the reactor through a showerhead at the rate of 100 sccm. Reactor
9 pressure was 10 Torr. Five minutes of processing in this manner
10 produced an amorphous layer consisting essentially of aluminum nitride
11 which was 1300 Angstroms thick. Resistivity in the layer was some
12 value greater than 1000 microhm-cm. Oxygen content was determined
13 to be 0.1%, with carbon content being below the detection limit of the
14 analysis tool, namely a carbon content of less than 1%.

15 The invention contemplates DRAM circuitry comprising a capacitor
16 dielectric region formed by aluminum nitride layer deposition in
17 accordance with the above and other methods. Referring to Fig. 1, a
18 wafer fragment 10 comprises two memory cells, with each comprising a
19 memory cell storage capacitor 12 and a shared bit contact 14.
20 Capacitors 12 electrically connect with substrate diffusion regions 18
21 through polysilicon regions 16. Diffusion regions 18 constitute a pair
22 of source/drain regions for individual field effect transistors. Individual
23 storage capacitors 12 comprise a first capacitor electrode 20 in electrical
24 connection with one of a pair of source/drain regions 18 of one field

effect transistor, and a second capacitor electrode 24. A capacitor dielectric region 22 is received intermediate first capacitor electrode 20 and second capacitor electrode 24. Region 22 comprises aluminum nitride, preferably deposited for example by the method described above.

Preferred as shown, region 22 contacts each of first capacitor electrode 20 and second capacitor electrode 24, and preferably consists essentially of aluminum nitride. A native oxide might form on the facing surfaces of at least one of first capacitor electrode 20 and second capacitor electrode 24, whereby the capacitor dielectric layer region would then consist essentially of aluminum nitride and native oxide in one preferred embodiment. The aluminum nitride of capacitor dielectric layer region 22 is preferably substantially amorphous, and deposited to an example thickness less than or equal to 60 Angstroms. More preferred, is a thickness which is less than or equal to 50 Angstroms, with both being thinner than conventional oxide-nitride-oxide capacitor dielectric layers commonly used in much existing DRAM circuitry.

An insulating layer 26 is formed over second capacitor electrode 24. A bit line 28 of an array of bit lines is fabricated in electrical connection with bit contact 14. An array of word lines 30 is fabricated to constitute gates of individual field effect transistors to enable selective gating of the capacitors relative to bit contact 14.

Other aspects of the invention are described with reference to Figs. 2 through 4. Fig. 2 illustrates a field emission device in the form

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1 of field emission display 40 in fabrication. In the depicted example,
2 such comprises an electron emitter substrate 42 formed of a glass
3 plate 44 having a first semiconductive material 46 formed thereover.
4 Semiconductive material 46 might comprise either a p-type doped or an
5 n-type doped semiconductive material (such as, for example,
6 monocrystalline silicon). Emitters 54 are provided in electrical
7 connection with layer 46, and preferably comprise a second
8 semiconductive material, for example doped polycrystalline silicon.
9 Exemplary dielectric regions 50, such as borophosphosilicate glass, are
10 provided over material 46 and intermediate emitters 48. An electrically
11 conductive extraction grid 52 is provided over dielectric material 50 and
12 accordingly is outwardly of and spaced from emitters 48.

13 Referring to Fig. 3 and in one aspect of the invention, an
14 electrically insulative material 56, other than an oxide of silicon, is
15 provided at least in partial covering relation over emitters 48. Such is
16 an improvement over native oxide coverings, which both consume emitter
17 material and appreciably dull the emitter tips. Further in one
18 considered aspect of the invention, layer 56 constitutes at least a partial
19 covering comprising aluminum nitride relative to emitters 48. In the
20 preferred embodiment and as shown, layer 56 is provided to entirely
21 cover emitters 48 and is formed after formation of extraction grid 52
22 and also is formed on extraction grid 52. An example and preferred
23 deposition thickness for layer/covering 56 is from about 50 Angstroms
24 to about 150 Angstroms. A preferred process for depositing

1 covering 56 in a substantially conformal and non-selective manner is as
2 described above, utilizing ammonia and at least one compound of the
3 formula R_3Al , where "R" is an alkyl group or a mixture of alkyl
4 groups, at a temperature or less than or equal to about 500°C and a
5 reactor pressure of from about 100 mTorr to about 725 Torr. Such
6 a layer can be deposited to be sufficiently smooth to not significantly
7 adversely affect tip sharpness, and is a material which reduces the
8 effective work function of the emitter tips, thereby reducing the required
9 operating voltage.

10 Referring to Fig. 4, electron emission substrate 42 is joined with
11 an electron collector substrate 60. Such is shown in the form of a
12 transparent face plate comprising phosphors 62 formed on a luminescent
13 screen 64. Spacers 66 separate and support electron collector
14 substrate 60 relative to electron emission substrate 42. Electron
15 emission 78 from emitters 48 causes phosphors 62 to luminesce and a
16 display to be visual through face plate 60. Techniques for forming field
17 emission displays are described in U.S. Patent Nos. 5,151,061; 5,186,670;
18 and 5,210,472, hereby expressly incorporated by reference herein.

19 In compliance with the statute, the invention has been described
20 in language more or less specific as to structural and methodical
21 features. It is to be understood, however, that the invention is not
22 limited to the specific features shown and described, since the means
23 herein disclosed comprise preferred forms of putting the invention into
24 effect. The invention is, therefore, claimed in any of its forms or

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1 modifications within the proper scope of the appended claims
2 appropriately interpreted in accordance with the doctrine of equivalents.
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